Fraunhofer-Projekt EMMA und weitere Förderaktivitäten aus Sicht von GLOBALFOUNDRIES

28.9.2018 Forschungsfabrik Mikroelektronik Deutschland, Berlin

Dr. Sabine Kolodinski, Staff Project Management

Agenda

1. Fraunhofer IPMS- Projekt EMMA
2. Connection to IPCEI WIN FDSOI
3. Technical Highlights and upcoming Ideas

Agenda

1	Fraunhofer IPMS- Projekt EMMA
2	Connection to IPCEI
3	Technical Highlights and upcoming Ideas

28.08.2018

Globalfoundries &
Fraunhofer IPMS-CNT

EMMA
IPCEI MICROELECTRONICS

PROJECT MOTIVATION

EMMA: **Developing innovative materials, processes, components, and characterization methods for semiconductor technology integration**

PROJECT CONTENT

#	Topic
WP1	Designabhängige Charakterisierung des Einflusses der STI-Füllprozesse auf die chemischen, strukturellen und elektrischen Eigenschaften von p- und n-FET SOI Substrate
WP1	Untersuchung der Wechselwirkung von STI-CMP unter Berücksichtigung von Struktur- und Prozessparametern
WP2	Untersuchung des vertikalen Gatewiderstandes von MOSFETs in Bezug auf RF-Eigenschaften
WP2	Untersuchung des Einflusses von Hochfrequenzstress auf die Transistoreigenschaften (DC & RF)
WP3	Einfluss der Prozessführung zeitmodulierter Plasmaätzprozesse und Entwicklung von prozessbegleitenden in-situ Analysemethoden
WP3	Entwicklung schädigungsfreier Strukturierungsprozesse und abgestimmter Charakterisierungsmethoden für die Realisierung innovativer Devicekonzepte
WP4	Charakterisierung von ferroelektrischen Feldeffektransistoren auf Basis von HfO2
WP4	Entwurf und Charakterisierung von ferroelektrischen Speicherarrays im Megabit Maßstab
WP4	Materialentwicklung von dotiertem HfO2 zur Anwendung in nichtflüchtigen ferroelektrischen Speichern
WP5	Untersuchung des thermoelektrischen Effektes für die integrierte Anwendung von Energie-Harvesting, Kühlung bzw. Sensorik und Entwicklung von geeigneten Integrationsansätzen
WP5	Evaluierung des pyroelektrischen Effektes von HfO2 zur elektrokalorischen Temperaturmanipulation auf Chip-Skala
WP6	Design und Integration von dreidimensionalen Kondensatorbauelementen in das BEoL für decoupling Anwendungen
WP6	Design, Integration und Charakterisierung von CMOS-kompatiblen RF-Varaktoren und Antennen für on-chip Anpassnetzwerke unter Verwendung der nicht-linearen Eigenschaften des ferroelektrischen HfO2
WP6	Untersuchung der Interaktion von Abscheideprozessen dielektrischer Materialien und alternative Integrationsansätze für die Metallisierung höchstintegrierter Schaltungen
WP7	Untersuchung wesentlicher Prozesseinflüsse auf das Random Telegraph- und 1/f Rauschverhalten von FD-SOI Transistoren
WP7	Elektrische Charakterisierung von hochstrukturierten Transistoren und Schaltungen im RF/mmWave-Frequenzbereich und Mitwirkung bei der Optimierung

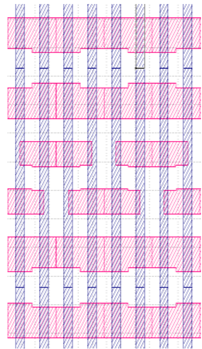
WP1 PROCESS AND DESIGN ENABLEMENT FOR DEVICE DIVERSIFICATION

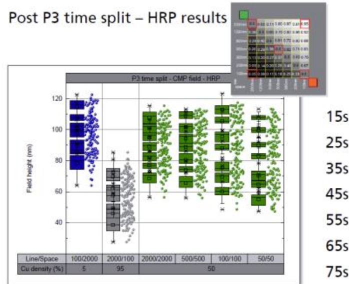
Layout and CMP process parameter influence

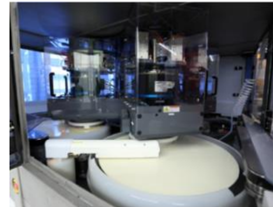
- Comparison between PWG and profilometry for planarity measurements
- Conversion of CMP tool for oxide-polish

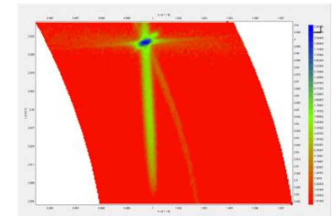
Oxide fill variations and design influence

- Principles of HR-XRD measurements
- Metrology options for SoI strain measurements and void detection





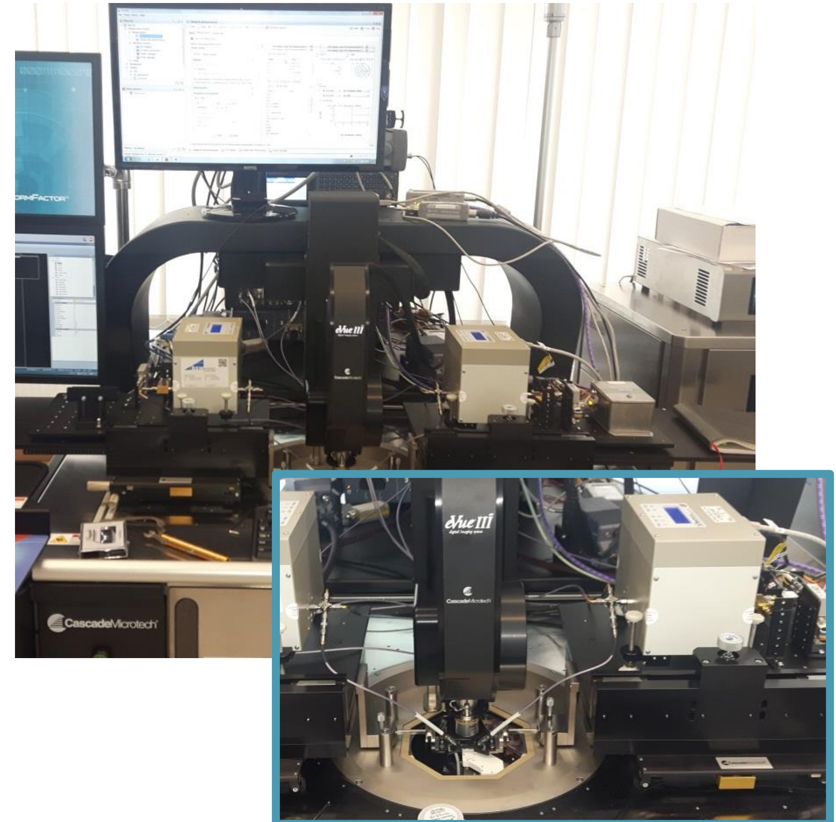




WP2 RF TECHNOLOGY ENABLEMENT

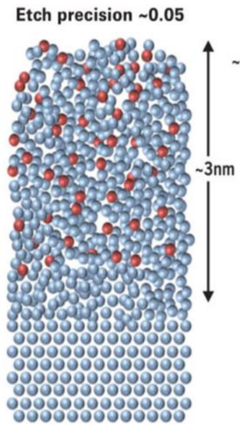
Advanced characterization of RF noise and reliability

- RF probestation ready to use
- RF equipment for analysis up to 110 GHz supporting
  - S-Parameters
  - load-pull
  - IMD
  - X-Parameters
  - Noise figure analysis



WP3 MULTIFUNCTIONAL ETCH ENGINEERING

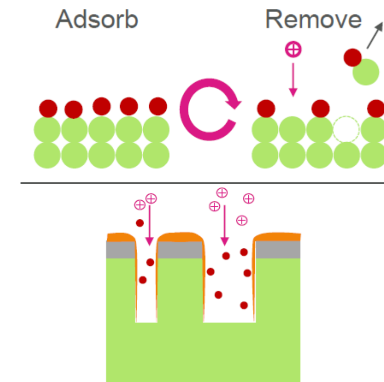
Testchip Development



- Additional functionalities for a testchip and characterization methods
  - Variations of size/pitch for characterization of process windows
  - Special designed test fields for inline characterization of damaged region (e.g. XPS, FTIR)
  - Additional contact level for improved electrical characterization

In-situ characterization

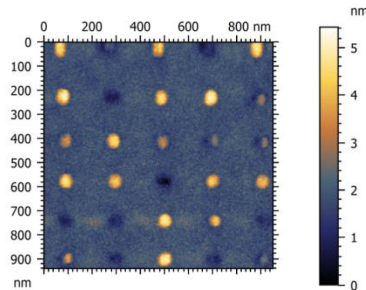
- Matching with Fab1 processes and in-situ methods

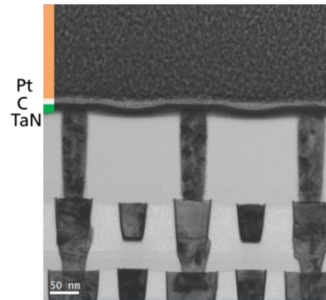


WP4 NEXT GENERATION NVM TECHNOLOGY

BEOL Integration of NextGen eNVM

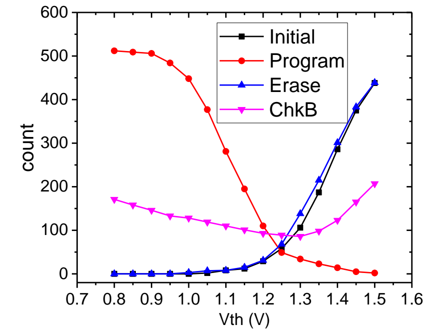
- Characterization of W plugs protrusion
- Ultra smooth TaN BE planarization





NVM-Array Characterization

- Testchip characterization environ-ment
- Establishing basic functions (package test)



PXIe testsystem

WP5 TEMPERATURE SENSING & MANIPULATION

Pyroelectrics

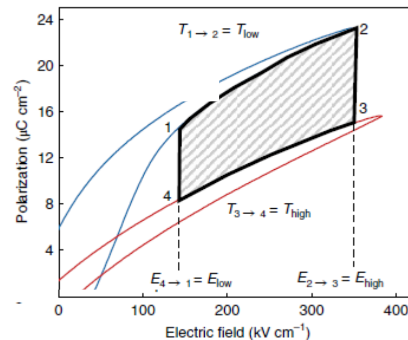
Determination of pyroelectric coefficient in Si-doped HfO_2 and $ZrHfO_2$ based on test structures for electrocaloric cooling

Thermoelectrics

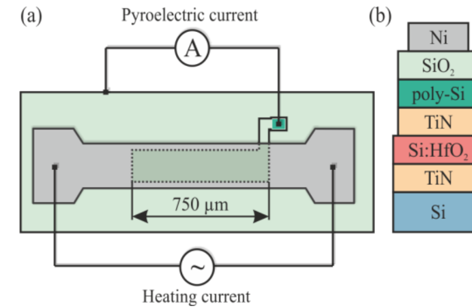
Study on existing integration concepts and CMOS-compatible materials with focus on metal oxides and silicides

Enhancing the material performance ZT by optimizing the adversely interdependent electrical resistivity, Seebeck coefficient, and thermal conductivity

Electrocaloric cooling cycles:



Pandya et al., 2018

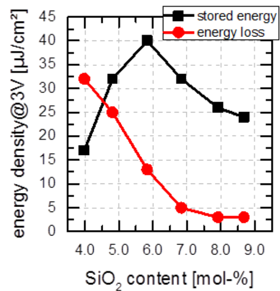


Mart et al., 2018

WP6 VAS ENABLEMENT

MIM and Varactor Development

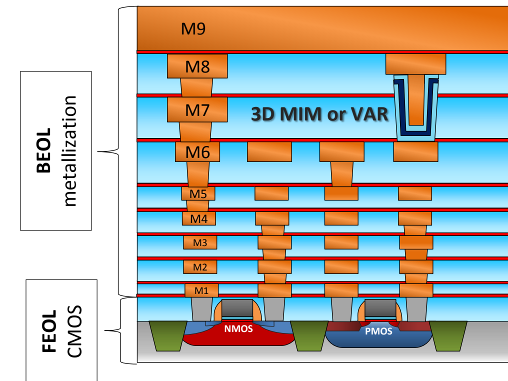
- Concepts on functional materials and device integration
  - Reliability tuning of ZrO_2 by doping and interface engineering
  - Antiferroelectric and ferroelectric material with optimized capacitance maximum to operation voltage
  - 3D integration of capacitors and varactors for capacitance enhancement



K. Kühnel, WODIM 2018

BEoL Development

- CVD tool matching with GF-Fab1 processes

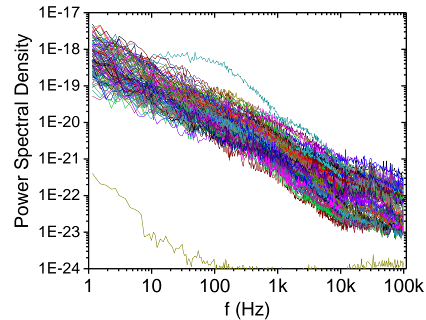


WP7 ADVANCED CHARACTERIZATION

RTN, Broadband 1/f noise characterization

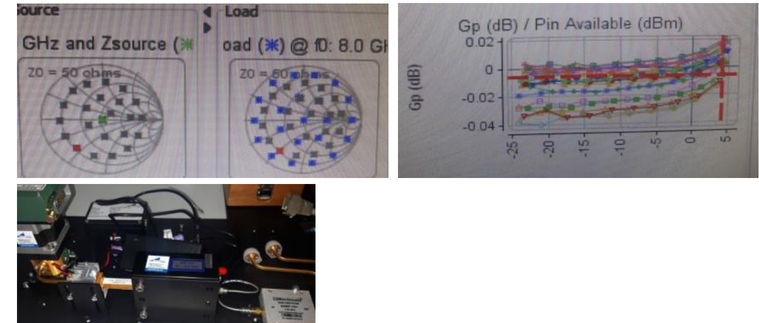
- I/f characterization platform tests on GF HW

Proplus System



Reliability & RF Characterization

- HCI qualification
- RF / mmWave and loadpull setup on GF hardware



THANK YOU!

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Funded by:

Agenda

1 Fraunhofer IPMS-Projekt EMMA

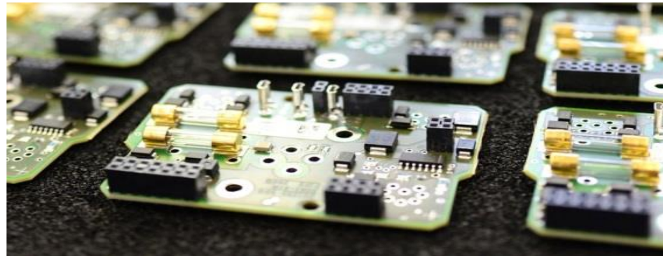
2 Connection to IPCEI WIN FDSOI

3 Subsidy compliance

4 Backup

IPCEI – connecting Europe's Microelectronic industry and creating new subsidy opportunity in EU

IPCEI on Microelectronics – 2017-2020



- New, untested subsidy program for "Important Projects of Common European Interest" (IPCEI) launched by EU Commission
- IPCEI project for Microelectronics set up to support Micro- and Nanoelectronics Manufacturing in the Supply Chain and to strengthen European industries in that sector
- **Major German Partners: Bosch, Infineon, Zeiss, X-Fab, GF**
- **German project volume 4.77 bn€**
- **German Fed Govt: Budgets of 1 bn€ subsidies**

Key Project Details

- GF participates in **subproject FDSOI:**

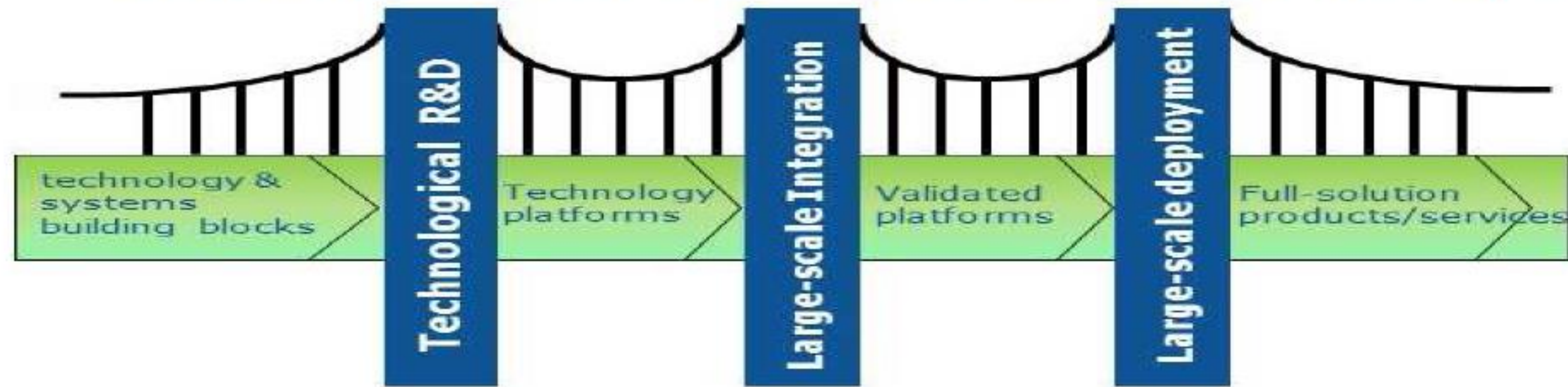
  Development and industrialization of innovative FDSOI-technology
  Enhancement of 22FDX technology, adding eNVM – MRAM//FeFET, HV and RF)
  Development of FDSOI-ecosystem (foundational and complex IP)
  Industrialization of 22 FDX technology

- **Project duration:** 15.1.2017 until 31.12. 2020
- **Project Partner:** STM (Fr), Soitec (Fr), X-FAB (Fr), Cologne Chip (Ge), RacyICs (Ge)

European Commission

From R&D to the deployment and investment needs

LETI is a key actor in: ECSEL pilot lines, the planned IPCEI, IoT pilots, …



Basic and applied research (TRL 2-5)
- Horizon 2020
- National and regional programmes

Development of platforms, scaling, experiments, pilot lines (TRL 5-8)
- H2020, Industry Member States

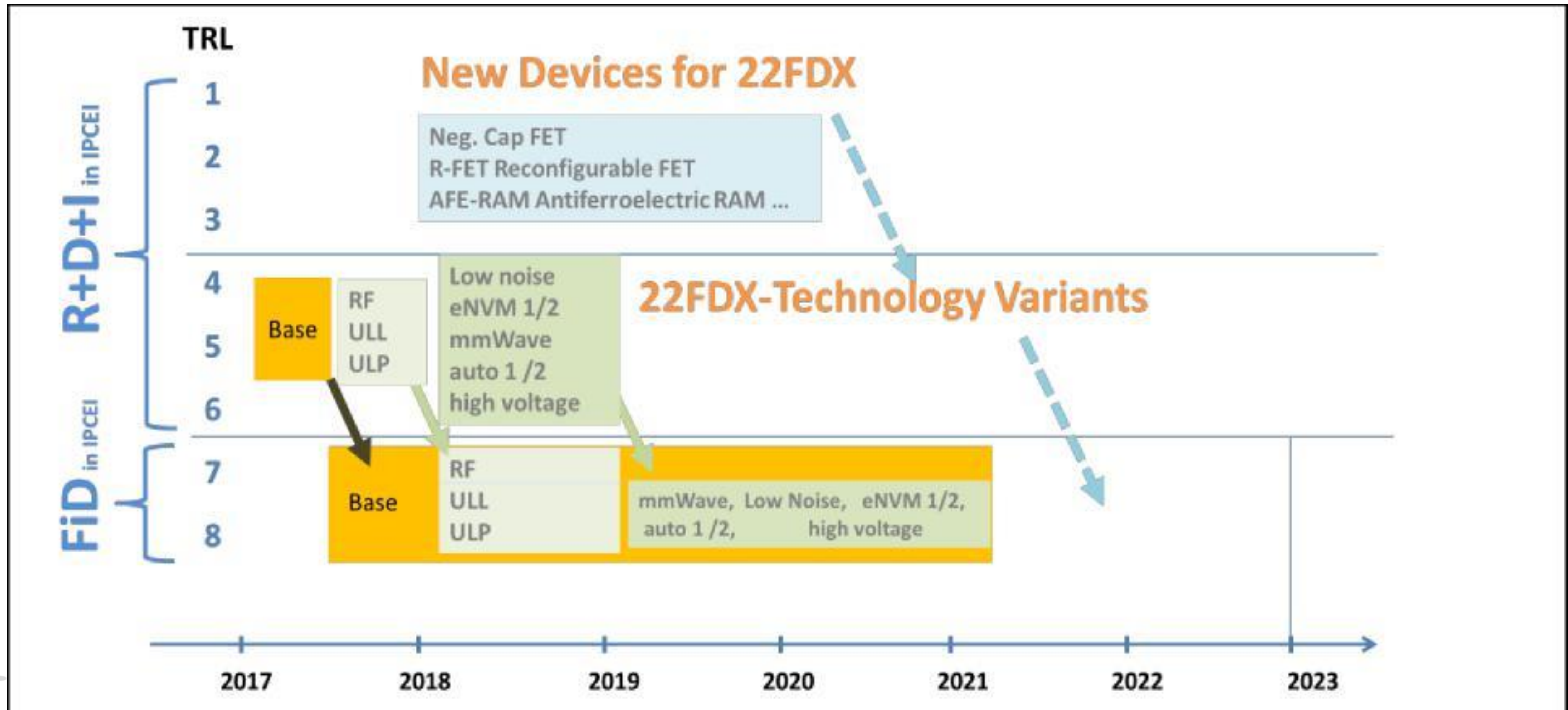
Deployment (TRL 8-9)
- Member States (state aid, **IPCEI***)
- Industrie

Investment needs x 10 x 10

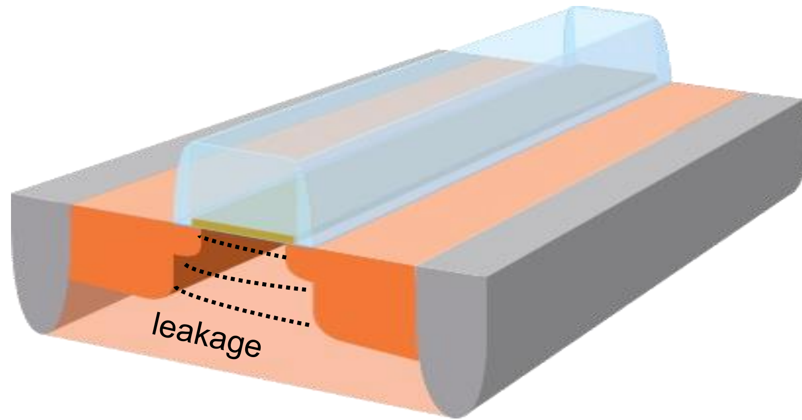
Commitment from PPPs essential at every stage

* IPCEI, Important Projects of Common European Interest

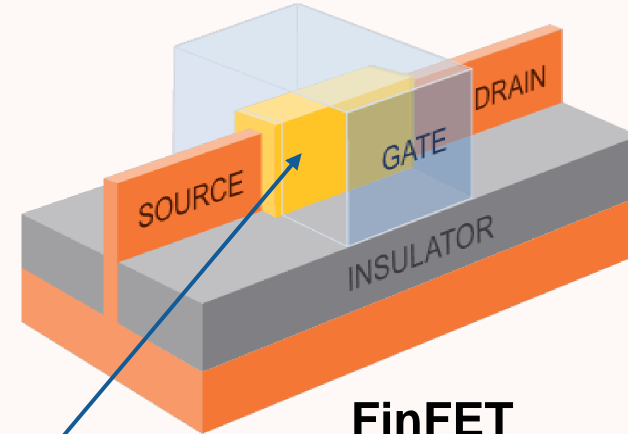
Scope of IPCEI WinFDSOI



Overcoming the limitations of short-channel effect in bulk CMOS

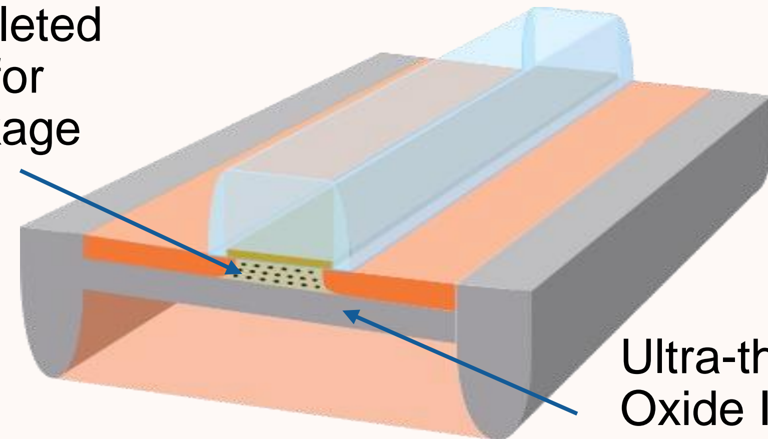


Bulk CMOS



FinFET

Fully Depleted Channel for Low Leakage

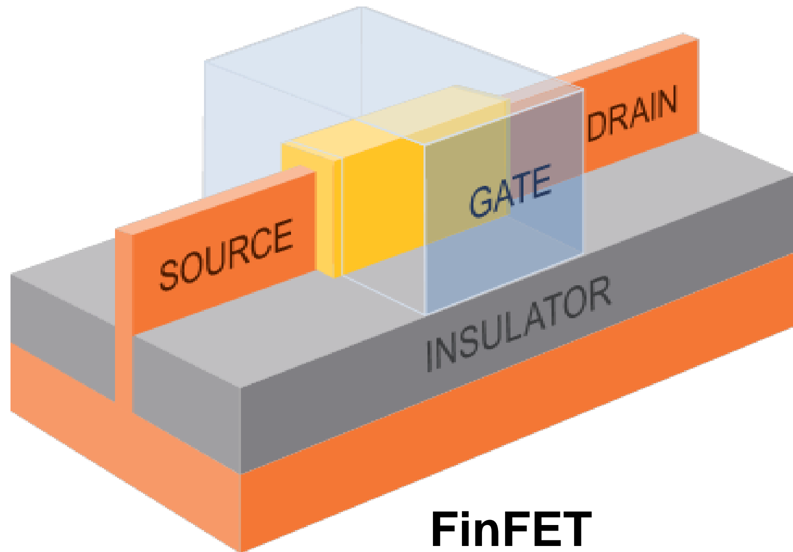


Ultra-thin Buried Oxide Insulator

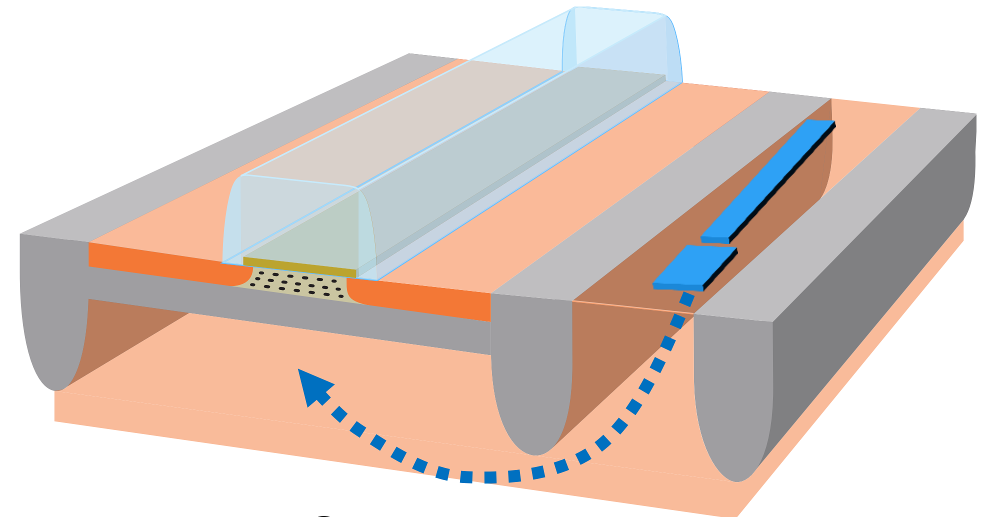
FD-SOI

- The "traditional" approach of simultaneous T,ox and Lg scaling for constant field doesn't work below 28nm technologies
- Junction leakage and variability prevent proper control

If it's the same "trick", then what distinguishes FDSOI and FinFET?



FinFET

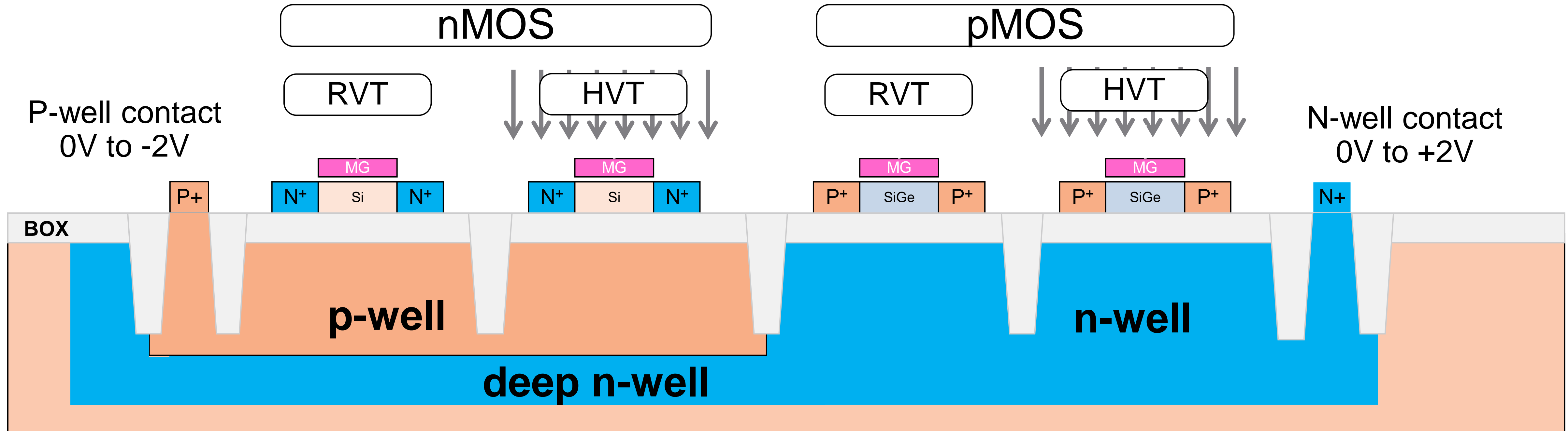


FD-SOI

- FinFET is the preferred technology for High-Performance computing because it can drive more current per area → vertical gate enables "double" gate area.
- FDSOI is the preferred technology for IoT, wireless, battery-powered etc. because it features something unique to reduce power consumption and leakage → **Backgate biasing**

Reverse Backgate Bias (RBB)

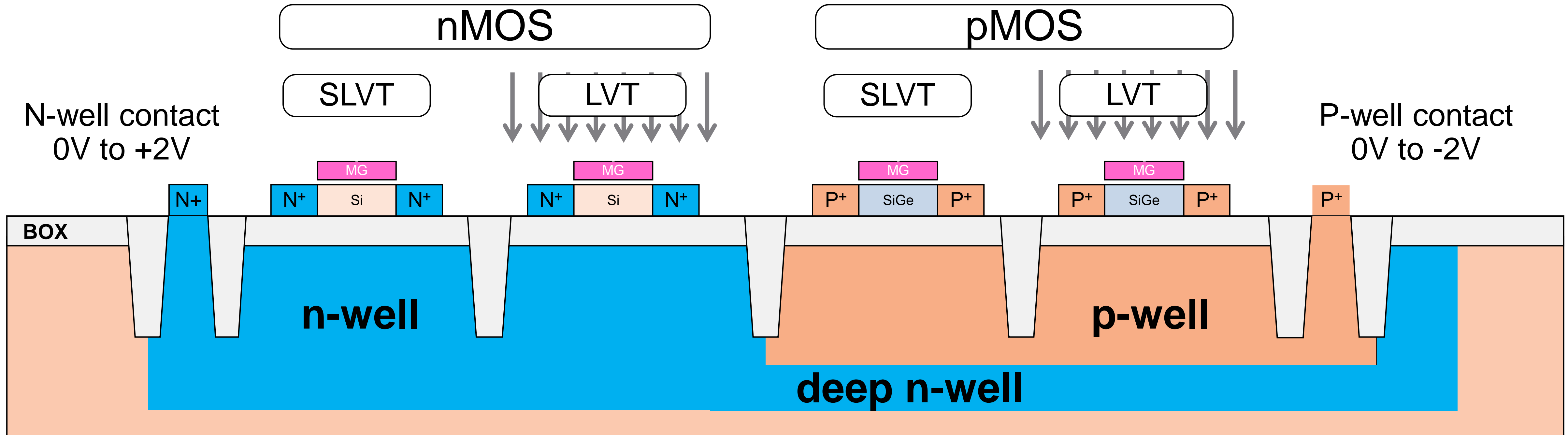
Conventional Well – RVT/HVT



- RVT/HVT are swappable post place-and-route without area scaling impact
- Full RBB capability with standard well scheme
- Gate length sizing for additional V_{TH}/I_{OFF} control

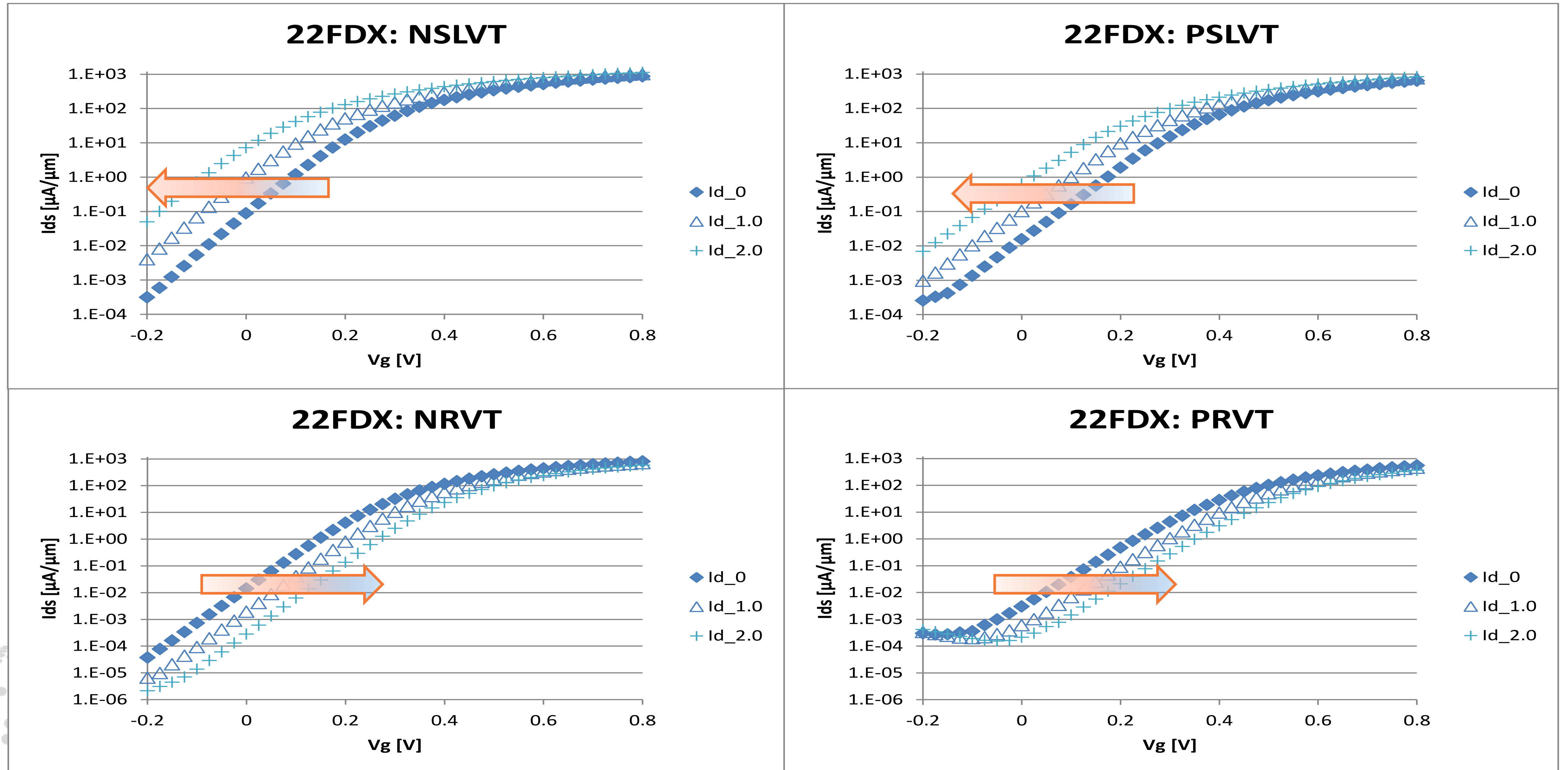
Forward Backgate Bias (FBB)

Flip Well – SLVT/LVT

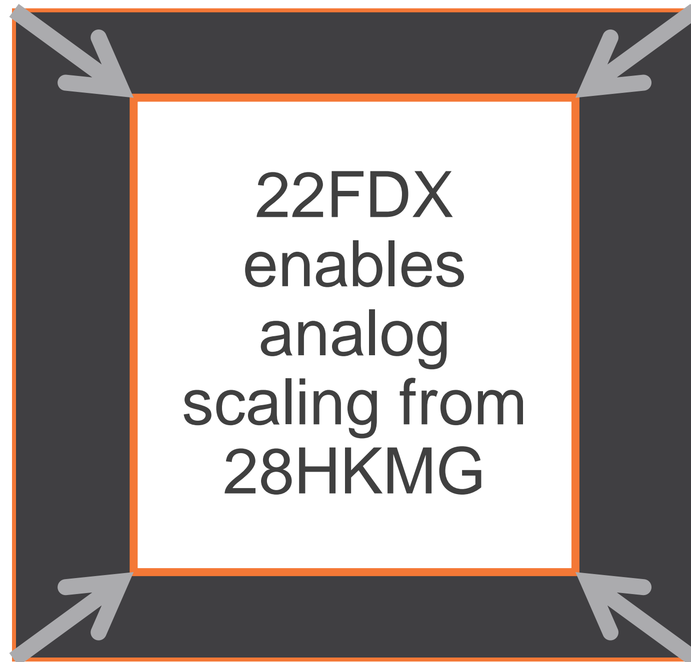


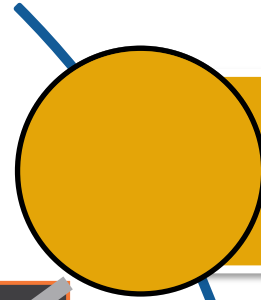
- SLVT/LVT are swappable post place-and-route without area scaling impact
- Full FBB capability with flip-well scheme
- Gate length sizing for additional V_T/I_{OFF} control

Performance increase or leakage reduction by backgate biasing (flip & conventional well)



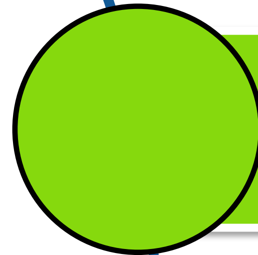
FDX™ Differentiation: Analog design scales in 22FDX…



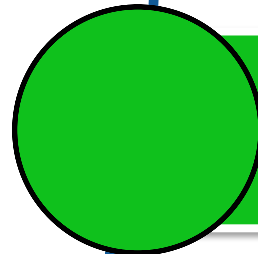


Short channel effects (DIBL, Velocity sat., channel-length modulation)

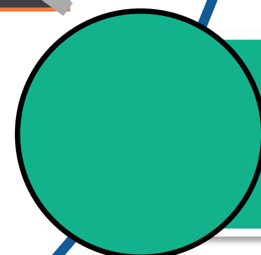
Negligible in 22FDX due to ultra-thin channel, i.e. s-d to bulk depletion region is negligible vs. gate length



Lower Mismatch due to un-doped channel eliminated random dopant fluctuation and field lines have tight distribution, i.e. require 4x larger device in 28nm to match 22FDX



Flicker Noise – Lower due to absence of channel doping & pocket implants, requires 5x larger device in 28HKMG to equal 22FDX noise characteristic



Higher gain for same power due to higher effective channel mobility (i.e. Gm) & lower Gds

Highlight: 22 FDX-devices

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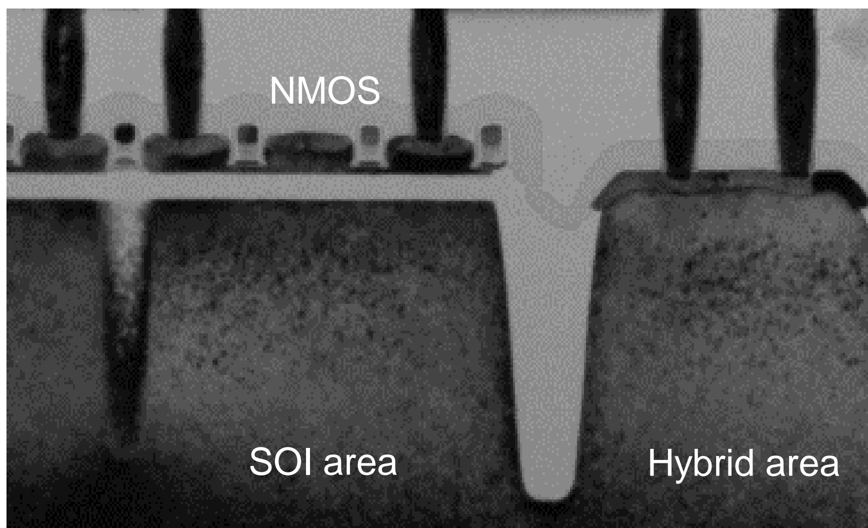

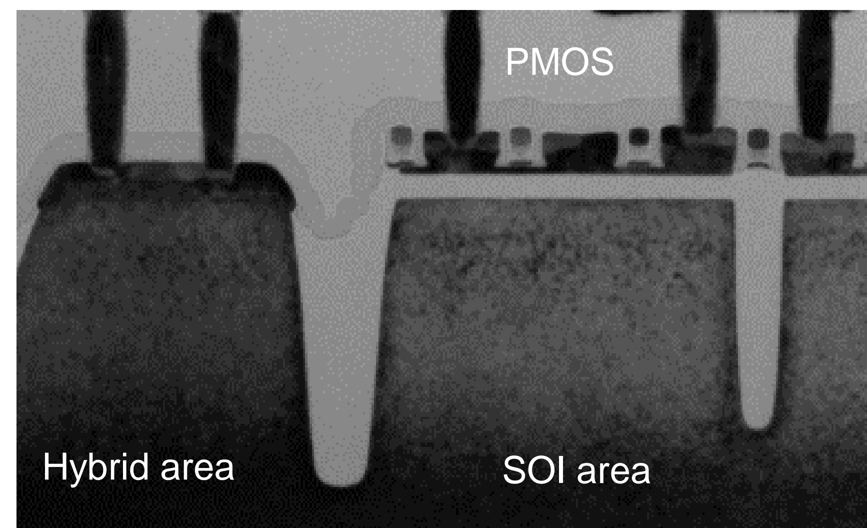

Device	SOI	Substrate	Comment
SG transistors	X		4 V_{TH} flavors for logic
EG transistors	X		2 V_{TH} flavors
Bitcell's	X		HD, HC, LV, ULV, ULL, Two-port
Resistors	X	X	Poly, diffusion, well
BJT		X	
Varactors		X	
eFuse		X	
Diodes		X	
RF devices	X	X	Includes also inductors, APMOMs etc.

- Active Devices in SOI, passives in substrate (hybrid)
- "Traditional" suite of transistors and passives is being offered

22FDX® In the News !

STMicroelectronics Selects GLOBALFOUNDRIES' 22FDX to Extend Its FD-SOI Platform and Technology

"The cost-effective performance and benefits of GF's 22FDX platform, coupled with ST's extensive design experience and IP base in FD-SOI, will enable our customers with unparalleled value for power, performance and cost." Joël Hartmann, EVP, STMicroelectronics

GLOBALFOUNDRIES Announces Availability of mmWave and RF/Analog on Landing FDX™ FD-SOI Technology Platform

Technology solution delivers 'connected intelligence' to next generation high-volume wireless and IoT applications with lower power and significantly reduced cost

GLOBALFOUNDRIES Announces Industry's Most Advanced Automotive-Qualified Production FD-SOI Process Technology

22nm FD-SOI (22FDX®) technology platform has been certified to AEC-Q100 Grade 2 for production.

GLOBALFOUNDRIES Announces Availability of Embedded MRAM on Leading 22FDX® FD-SOI Platform

Advanced embedded non-volatile memory solution delivers 'connected intelligence' by expanding SoC capabilities on the 22nm process node

GLOBALFOUNDRIES and VeriSilicon To Enable Single-Chip Solution for Next-Gen IoT Networks

Integrated solution leverages GF's 22FDX® technology to decrease power, area, and cost for NB-IoT and LTE-M applications

Arbe Robotics Selects GLOBALFOUNDRIES for its High-Resolution Imaging Radar to Enable Safety for Autonomous Cars

Arbe Robotics' proprietary chipset leverages GF's 22FDX® technology to deliver industry's first real- time 4D Imaging Radar for level 4 and 5 autonomous driving

GLOBALFOUNDRIES Strengthens 22FDX® eMRAM Platform with Evaderis' Ultra-low Power MCU Reference Design

Co-developed technology solution enables significant power and die size reductions for IoT and wearable products

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Integrated Character of IPCEI WIN-FDSOI

- Partner RACYICs: modular platform-SoC for IoT and industry 4.0 applications and implement it in 22FDX technology
- Partner Cologne-Chip: Field Programmable Gate Arrays with 22-FDX (unique in EU)
- Partner SOITEC: Substrates
- Partners ZEISS & AMTC: Advanced Methods for Chip Manufacturing Enhancement
- Spillover to 17 subcontracts

Subcontracts grouped into topics enhancing impact of 22-FDX

Group A: Add on-functionalities and processes for 22-FDX:

FhG IPMS, NaMLab, FhG IMS, FhG IKTS

Group B: Managing the Performance/ Reliability-Trade-off of HKMG/ Inclusion of transient measurements

FhG IPMS, NaMLab, AQ Computare, TU DD (Prof. Weber), Bergakademie Freiberg (Prof. Heitmann)

Group C: 5G and radar complete system showcases including char. of packages with respect to E/B field
TUDD, Profs Ellinger/ Mayr/ Bock, FhG IZM Assid & FhG ENAS

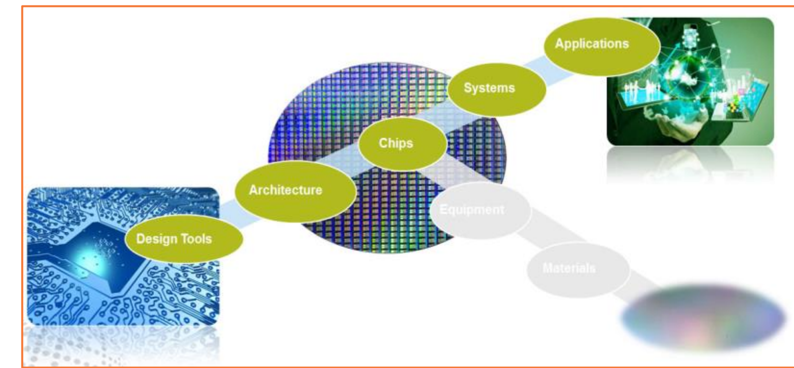
Group D: Additionel IP-elements for 22-FDX

FMC, FhGEAS/IIS, Extoll, Dreamchip

Group E: RF and mm-Wave characterisation and modelling & Reliability

GWD of TU DD (Prof. Schröter) HTW-DD (Prof. Klix), FhG IPMS

Spill-over Beyond IPCEI: Application based value chain



SoCs for Automotive:

- Robert Bosch
- Audi AG
- IFX

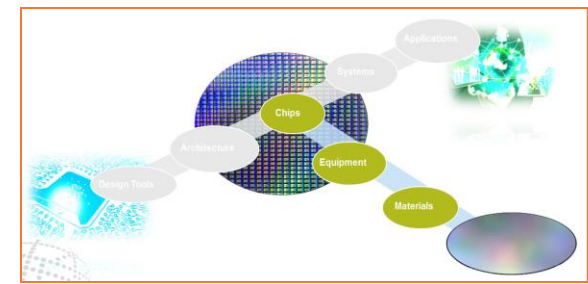
SOCs for IoT:

- TU Dresden, Technolution (NL), IDT (Ge), IMEC (Be) and Leti (Fr), ST Microelectronics (Fr)
- Fraunhofer
- Soitec
- ECSEL project OCEAN12
  - R&D-work (Soitec)
  - design IP R&D (Robert Bosch, Kalray, others)
  - Technologies: STM – Crolles; GF Dresden

SOCs for security:

- Ferroelectric Memory Company (FMC), Infineon, ST Microelectronics, NXP
- Coinbau co-operation on chips for Blockchain farms in Iceland

Spill-over Beyond IPCEI: Materials based value chain



Cooperation with

- ASML on lithography equipment and lithography development
- SILTRONIC in addition to Soitec for wafer-materials

- *Local* HSEB developed equipment to measure maps of different layer thicknesses of substrates
- AMAT: improvements of implant-, etch-, and deposition-equipment.
- LAM: EPI-, plasma-, and etch-equipment
- Air Liquide
- Intelligent Fluids: cleaning chemistry for semiconductor processing.

Further Spill-Over: Cooperation with universities

- Technical University of Dresden
- University of Wuppertal
- Technical University of Berlin
- University of Twente (Netherlands)
- Technical University of Delft (Netherlands)
- University of Oulu (Finland)
- KU Leuven (Belgium)
- University of Manchester (United Kingdom)
- ETH Zürich (Switzerland)
- Chalmers University (Sweden)
- Lund University (Sweden)

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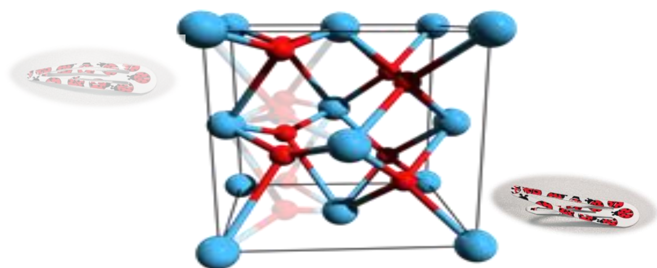
Agenda

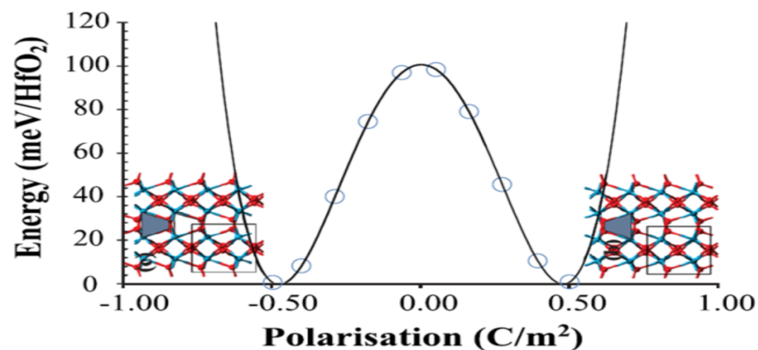
1. Fraunhofer-IPMS Projekt EMMA
2. Connection to IPCEI WIN FDSOI
3. Technical Highlights and upcoming ideas

Ferroelectric FET as eNVM

a simple system – VT shift through polarization

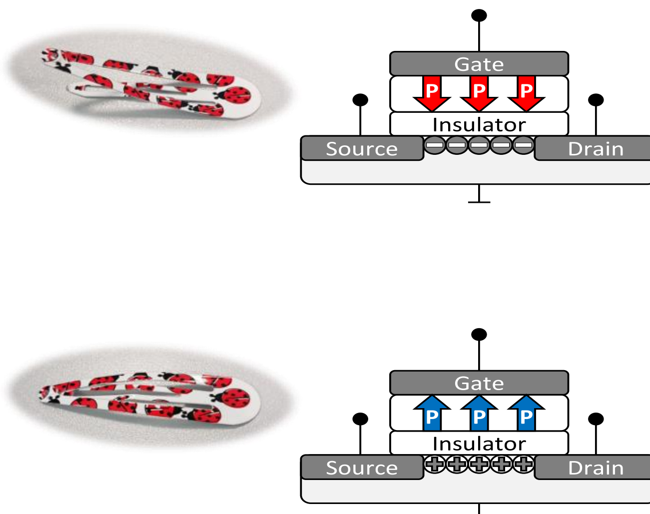
Cristal with two optional atom positions:



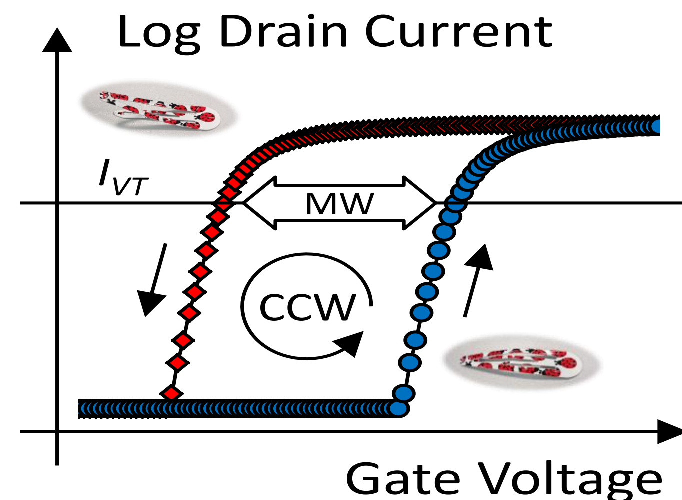


S. Clima et al., Appl. Phys. Lett., 2014

Simplified operation:



(One) figure of merit:
The memory window (MW)



Programmed / low V_T state

Erased / high V_T state

Switching by voltage only, with the speed of sound
(over film thickness of ~10nm ~ ps switching speed)

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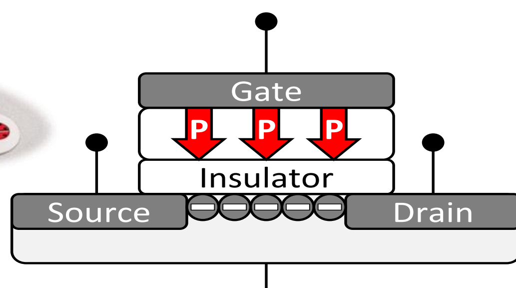
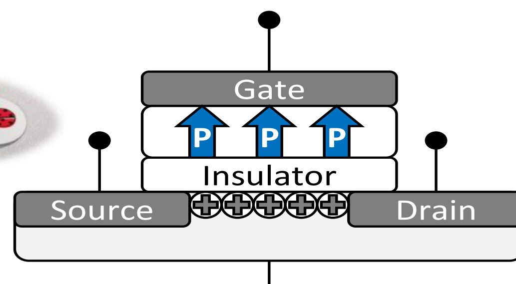
Charge Trapping vs. Polarization

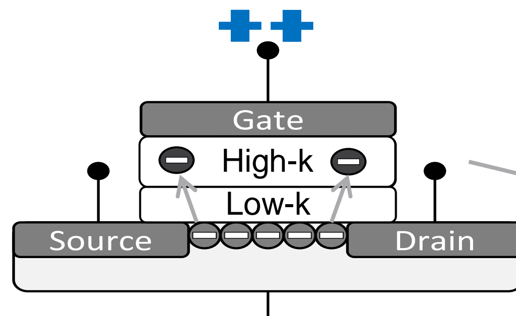
two counteracting phenomena

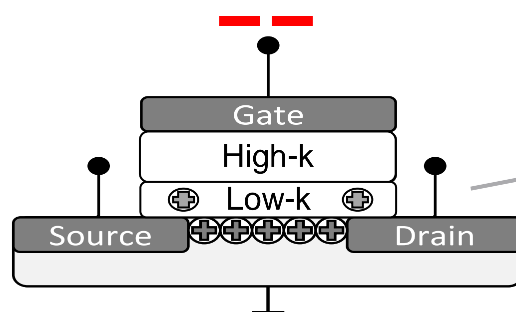
Dipole Orientation:



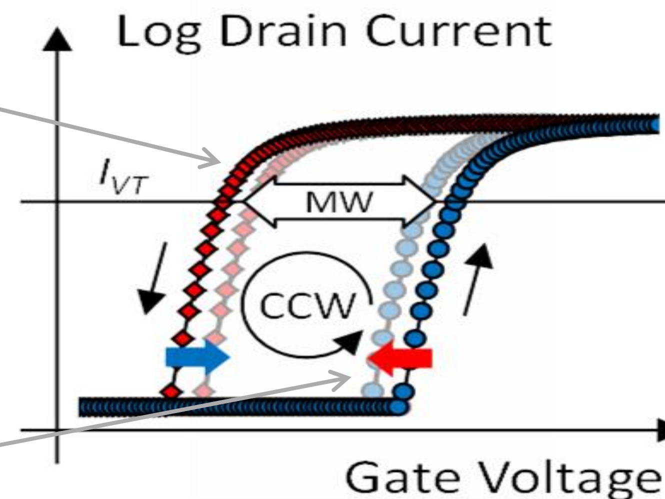


Charge Trapping:





MW-Reduction:



High programming fields provoke counteracting charge trapping – closing the MW in the opposite direction.
The ferroelectric crystal is not degrading by theory, yet the trap density and trap depth ages with operating lifetime, depending on operation conditions, and closes the MW at some point.

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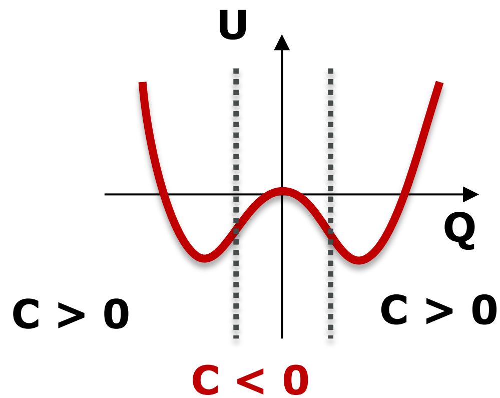
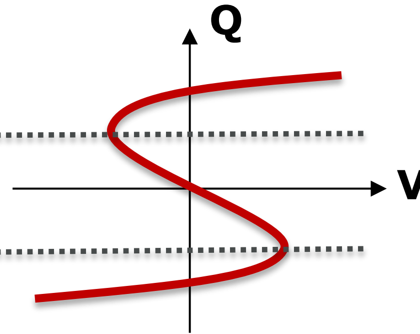
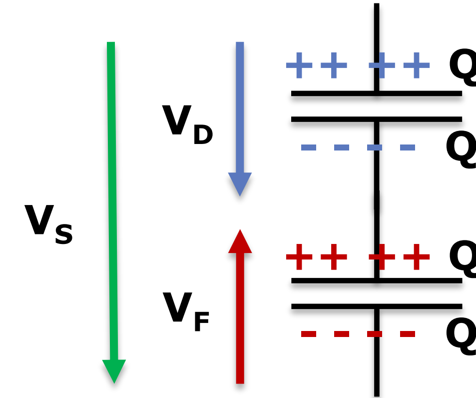
NCFET – steep slope by negative capacitance effect

Ferroelectric Landau model:

$$U_F = \alpha Q^2 + \beta Q^4 + \gamma Q^6,$$







Total Capacitance:

$$C = \frac{C_D C_F}{C_D + C_F} > C_D, \quad \text{if } |C_F| > C_D$$

$$C_F < 0$$

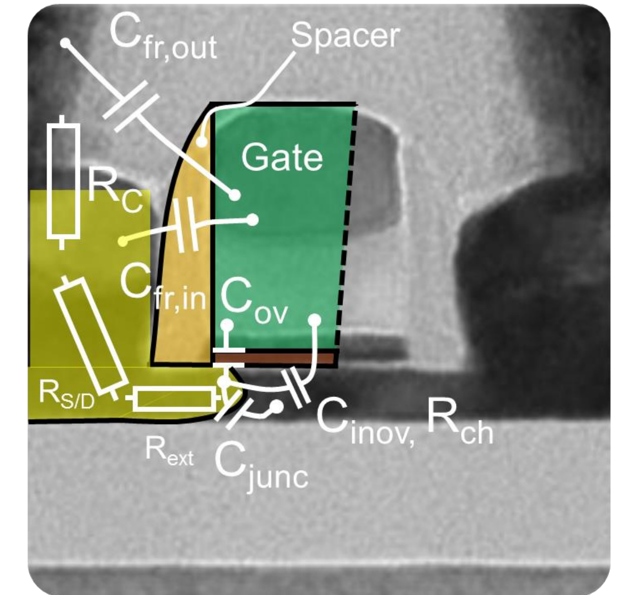
$$S = \frac{\ln(10) \cdot k \cdot T}{q} \cdot \left(1 + \frac{C_{Depl}}{C_{Ins}}\right)$$

- **Negative differential capacitance (NDC)** can exist in ferroelectric phase material
- Negative differential capacitance can be **stabilized by a series capacitor**
- The total **capacitance might become larger** than the pure dielectric capacitance
- Negative capacitance in transistor gate stack will lead to **reduced sub-threshold swing**

namlab confidential

Effect of parasitic capacitances on RF and mm-Wave performance

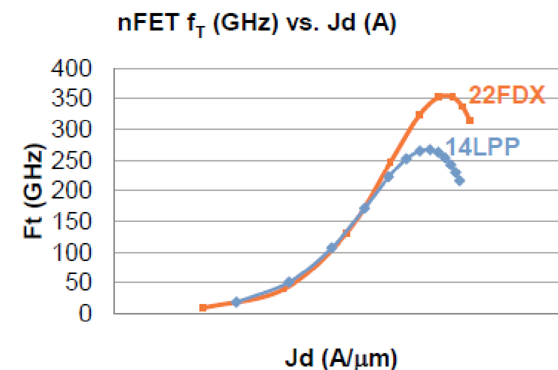
Element	Cgd	Cgg	gmsat	gds	ft	fmax*
Lg reduction	⇔	↘↘	↗↗	↗↗	↗↗	↗
Tinv reduction	⇔	↘	↗	⇔	⇔	⇔
PC height	⇔	⇔	⇔	⇔	⇔	⇔
EPI Thk reduction	↘	↘	↘	↘	↗	↗
Spc + RTA	Adjusted at same Vt and SCE				⇔↗	⇔↗

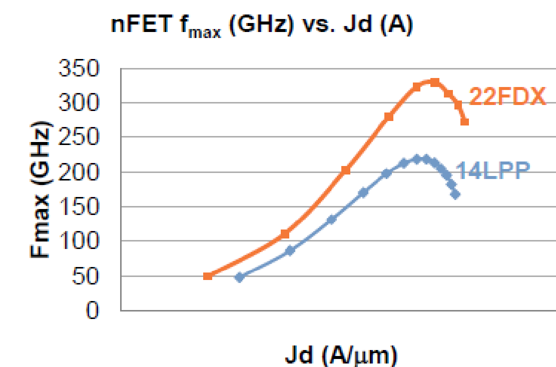


RF-FET	22-FDX n-Kanal-FET	22-FDX p-Kanal-FET
F_T(GHz)	350	270
F_{max}(GHz)	400	300

22FDX® Outperforms FinFET for f_T/f_{Max}

Silicon data - Outperforms FinFET and other advanced nodes for f_T/f_{MAX}





- nFET results comparing W=0.5um 22FDX to 12 Fin 14LPP

Aussagen zu Truly Complementary Design
Prof. Dr. F. Ellinger

- Wenn es gelingt pFEts gleich schnell wie nFETs zu machen, wird dies in der Schaltungstechnik zu einem Paradigmenwelchsel führen, da nun wesentlich bessere Performanzen und neuartige verbesserte Schaltungsarchitekturen möglich sind:
- Im Laufe des Projektes werde ich deshalb wohl mein Skript und auch mein Springer-Lehrbuch umschreiben müssen, was ich sehr gerne tun werde!
- Globalfoundries hat sehr vielversprechende Ideen entwickelt, um dieses seit Jahrzehnten ungelöste Problem zu lösen!

Fraunhofer EMMA & IPCEI Funding lead to 22-FDX to Success

- Fraunhofer IPMS contributes with a PhD-Programme and major activities to IPCEI project on the industrialisation of 22-FDX. Further subcontracts complete the Design ecosystem, add-on functionalities and new innovative devices.
- FDSOI delivers highest performance at low operating power.
- R&D Add-On-Functionalities: logic, analog, RF, auto and e-NVM for SoCs at the edge of ArF-Immersion Lithography.
- First industrial Deployment is included to bridge the Valley of Death.
- Spill-Over to RTO, SMEs and start-up in the 22-FDX-ecosystem is generated.
- GF Fab One will enhance the European ecosystem for highest performancing Chips with lowest operating power for new markets IoT, automotive, security etc.

Thank you very much!

Gefördert durch:

Bundesministerium
für Bildung
und Forschung

Bundesministerium
für Wirtschaft
und Energie

aufgrund eines Beschlusses
des Deutschen Bundestages

Europäische Union

Europa fördert Sachsen.

Diese Maßnahme wird mitfinanziert durch Steuermittel auf Grundlage des von den Abgeordneten des Sächsischen Landtags beschlossenen Haushaltes.